In The Claims:

Claims 1-13 (canceled)

14. (currently amended) A MOS transistor, comprising:

a substrate;

a gate dielectric layer on the substrate;

a stacked gate on the gate dielectric layer, comprising, from bottom to top, a first barrier layer, an interlayer, a work-function-dominating layer, a second barrier layer and a poly-Si layer, wherein the work-function-dominating layer comprises a metallic material, and the interlayer includes a material capable of controlling a crystal orientation of the work-function-dominating layer to adjust a work function of the work-function-dominating layer; and

a source/drain in the substrate beside the gate.

15. (canceled)

16. (original) The MOS transistor according to claim 14, wherein the interlayer includes a material capable of wetting a surface of the first barrier layer.

17. (original) The MOS transistor according to claim 14, wherein a thickness of the interlayer is smaller than a thickness of the work-function-dominating layer.

18. (original) The MOS transistor according to claim 14, wherein a thickness of the work-function-dominating layer is larger than a total thickness of the first and second barrier layers.

19. (original) The MOS transistor according to claim 14, wherein the gate dielectric layer comprises a high-K dielectric layer.

20. (original) The MOS transistor according to claim 14, further comprising:

a spacer on a sidewall of the gate; and

a pair of lightly doped drains in the substrate,

wherein the source/drain is in the substrate beside the spacer, and the lightly doped drains are in the substrate beside the gate connecting with the source/drain.